PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Pradeep Sindhu; Dennis C. Ferguson	Confirmation No.	4412
Serial No.:	10/004,536		
Filed:	October 31, 2001	Customer No.:	28863
Examiner:	Joseph E. Avellino		
Group Art Unit:	2143		
Docket No.:	1014-014US01/JNP-0074		
Title:	NETWORK ROUTER HAVING EMBEDDED MEMORY		

REPLY BRIEF

Board of Patent Appeals and Interferences
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

Dear Sir:

This is a Reply Brief to the Examiner's Answer mailed March 8, 2007. The Examiner's Answer raised a new ground of rejection, thus necessitating this Reply Brief.

Appellant's Appeal Brief was filed December 11, 2006 in response to the Final Office Action mailed June 16, 2006. The Notice of Appeal was filed on September 18, 2006. No fee is believed due. Please charge any deficiencies or credits to Deposit Account No. 50-1778.

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REAL PARTY IN INTEREST

The real party in interest is Juniper Networks, Inc. of Sunnyvale, California.

RELATED APPEALS AND INTERFERENCES

There are no related appeals and interferences.

STATUS OF CLAIMS

Claims 1-9, 11-20, 22-26, 28-32 and 34-35 are on appeal in this case. All claims are being appealed.

All claims stand rejected under 35 U.S.C. 103(a) as being unpatentable over Mathur (USPN 6,424,658) in view of Muller et al. (USPN 6,245,680).

In the Examiner's Answer, the Examiner raised a new ground of rejection and rejected all claims under 35 U.S.C. 102(e) as being anticipated by Bass et. al (USPN 6,460,120).

STATUS OF AMENDMENTS

No amendments have been filed subsequent to the Final Office Action mailed June 16, 2006 from which this Appeal has been made.

SUMMARY OF THE CLAIMED SUBJECT MATTER

A concise summary of independent claim 1, 9, 18, 24, 30 and 35 is provided within Appellant's Brief filed December. Per MPEP 1208, the Summary of the Claimed Subject Matter has been omitted from this Reply Brief.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. The first grounds for rejection to be reviewed on Appeal is the rejection of claims 1-9, 11-20, 22-26, 28-32 and 34-35 under 35 U.S.C. 103(a) as being unpatentable over Mathur (USPN 6,424,658) in view of Muller et al. (USPN 6,245,680).

2. The second grounds for rejection to be reviewed on Appeal is the rejection of claims 1-9, 11-20, 22-26, 28-32 and 34-35 under 35 U.S.C. 102(e) as being anticipated by Bass et al. (USPN 6,460,120).

ARGUMENTS

The First Ground of Rejection

Claims 1-9, 11-20, 22-26, 28-32 and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mathur (USPN 6,424,658) in view of Muller et al. (USPN 6,245,680).

With respect to the first ground of rejection, Appellant argues claims 1-9, 11-20, 22-26, 28-32 and 34-35 as a group, as set forth below. Appellant directs the Board to independent claim 1.

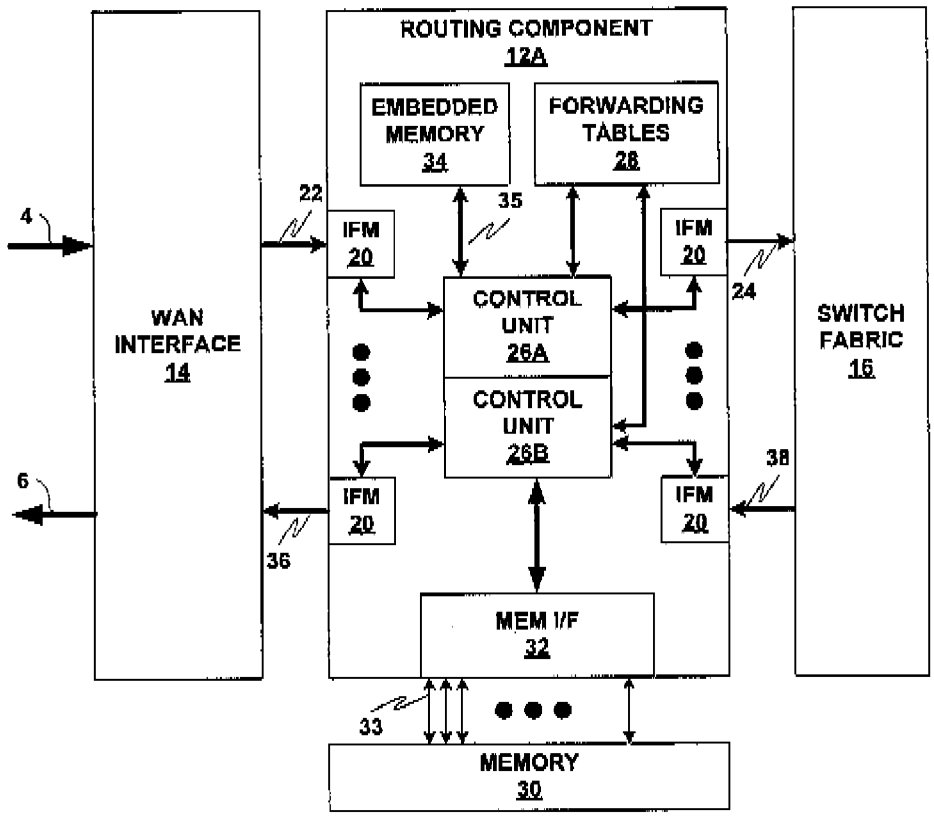
Claim 1

As discussed above, claim 1 is directed to a routing component within a router, the routing component comprising a first interface to communicate data with a network and a second interface to communicate data to a second routing component using a switch internal to the router. Claim 1 requires that the first interface and the second interface are integrated within a single integrated circuit. Claim 1 also requires that the routing component include an embedded memory within the integrated circuit, and a memory interface to couple the integrated circuit to an external memory.

Claim 1 further recites at least one control unit that receives data from the network via the first interface and accesses a forwarding table to determine a network destination for the data. Claim 1 requires that the control unit buffer the data using the embedded memory internal to the integrated circuit when the destination requires forwarding the data to the second routing component of the router using the switch. In addition, claim 1 requires that the control unit buffer the data in the external memory when the destination requires forwarding the data to the network via the first interface.

In this manner, the literal language of claim 1 is directed to a routing component in which data received from the network on the <u>same</u> interface (e.g., inbound packets from WAN interface 14) are buffered differently by using either embedded memory or external memory based on the particular destination to which the data is to be forwarded.

To illustrate this by way of example in reference to the present application, Appellant directs the Board to FIG. 2, reproduced below:



With respect to FIG. 2, the present application states that upon receiving an inbound packet via input link 4, control units 26A, 26B of routing component 12A may forward that inbound packet either directly to outbound link 6 via WAN interface 14 or to another routing component via internal switch fabric 16.[1] In this manner, in the described embodiment, a data packet received on the same interface (e.g., an inbound packet received from the network via link 4) may be forwarded directly back to the network as an outbound packet using a network interface (e.g., WAN interface 14) or forwarded to another routing component by the internal switch fabric 16. In this regard, when forwarding packets, control units 26 of routing component 12A actively make buffering decisions based on the destination for the particular data (e.g., packet). That is, as described at length in the application, data received from an interface, such as inbound packets received from the network, is buffered differently (i.e. using either embedded memory 34 or external memory 30) based on the destination specified within the packet.

For example, pg. 7, ll. 19-32 describes buffering network data within small, high-speed embedded memory 34 within the integrated circuit when it is determined that the network data is destined for a second routing component within the router. Conversely, pg. 7, ll. 5-18, describes buffering data within a large, external memory device 30 when it is determined that the data is destined for the network.

This feature of selecting between internal (i.e., on-chip) and external (i.e., off-chip) memory to buffer data based on a destination to which the data is to be forwarded is a requirement of claim 1. Claim 1 specifically requires that the at least one control unit buffer the data received from the network using the embedded memory internal to the integrated circuit when the destination requires forwarding the data to the second routing component of the router using the switch, and buffer the data from the network in the external memory when the destination requires forwarding the data to the network via the first interface. In this manner, the literal language of claim 1 is directed to a routing component in which data (e.g., inbound packets) received from the network on the same interface is buffered differently, i.e. using either internal or external memory, based on the particular destination to which the packet is to be forwarded.

In the Final Office Action, the Examiner argued that Mathur discloses a routing component having substantially all of the features of Applicant's independent claims, but acknowledged that Mathur utilizes only internal memory and does not disclose use of an external memory. With respect to these features, the Examiner cited Muller as disclosing a routing element that utilizes external memory. Based on the Mathur reference that describes using entirely internal memory and the Muller reference that describes using entirely external memory, the Examiner concluded that it would have been obvious to one of ordinary skill to modify the Mathur routing component in view of Muller to achieve Applicant's claimed invention.[2]

Mathur in view of Muller fails to teach or suggest a routing component having a control unit that buffers the data received from the network using the embedded memory internal to the integrated circuit when the destination requires forwarding the data to the

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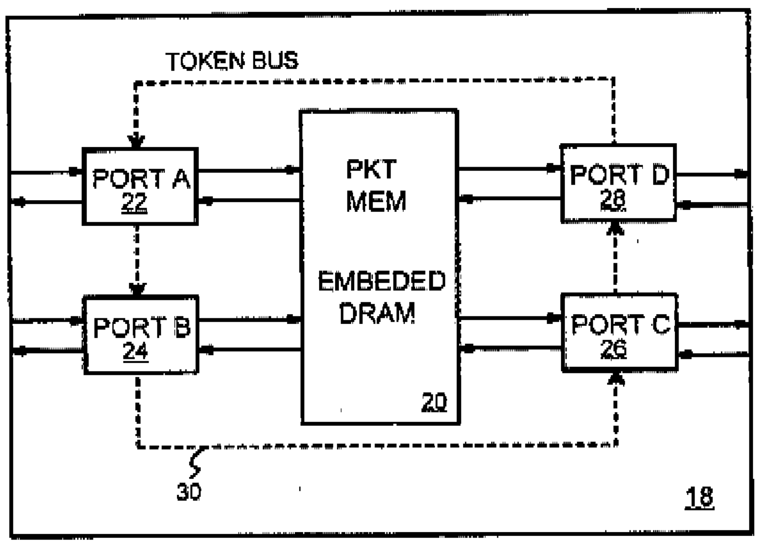
[1] Pg. 6, ln. 26-pg. 7, ln. 5.
[2] See Office Action pg. 3.

second routing component of the router using the switch, and buffers the data from the network in the external memory when the destination requires forwarding the data to the network via the first interface. For these or similar reasons, Mathur in view of Muller fails to teach or suggest the elements of independent claims 9, 18, 24, 30 and 35.

Mathur (USPN 6,424,658)

Mathur describes a store-and-forward network switch that uses an embedded dynamic-random-access memory (DRAM) packet memory. In particular, FIG. 2 of Mathur shows a network switch chip 18 that receives packets from one of four ports A, B, C, D and stores the packets in embedded DRAM packet memory 20. The network switch chip 18 transmits the stored packets out to one or more of the four ports A, B, C, D. The following is a reproduction of FIG. 2 of Mathur:



As shown in FIG. 4, Mathur makes clear that <u>all</u> packets forwarded between ports 22-28 are stored in embedded packet memory 20. For example, at col. 6, ll. 3-7, Mathur specifically states the following:

> *Port logic 22, 24, 26, 28 are bi-directional ports to a network node connected to a computer, peripheral, LAN segment, or other network equipment such as another switch, router, repeater, bridge or hub. Packets may be input or output from any port. When a packet is received by port logic 22, 24, 26, 28, it first writes the packet into embedded DRAM packet memory 20.*

Thus, as stated above and illustrated in FIG. 2 (above), Mathur teaches a switch in which packets forwarded between any of the four interface ports 22-26 are buffered within an embedded packet memory 20 regardless of the forwarding operation. With respect to buffering packets, no regard is given to the destination of the packet. In fact, no decision is made whatsoever, let alone with respect to which type of memory to use to buffer the packet. All packets forwarded between ports 22-28 are stored in embedded packet memory 20 regardless of destination or any other criteria. No controller determines destinations for packets received from the same interface and then buffers the packets differently based on the respective destinations.

Muller et al. (USPN 6,246,680)

Muller describes a highly integrated multi-layer switch element. According to Muller, the switch element includes multiple ports for transmitting and receiving packets over a network. FIG. 2 of Muller illustrates the described switch element:

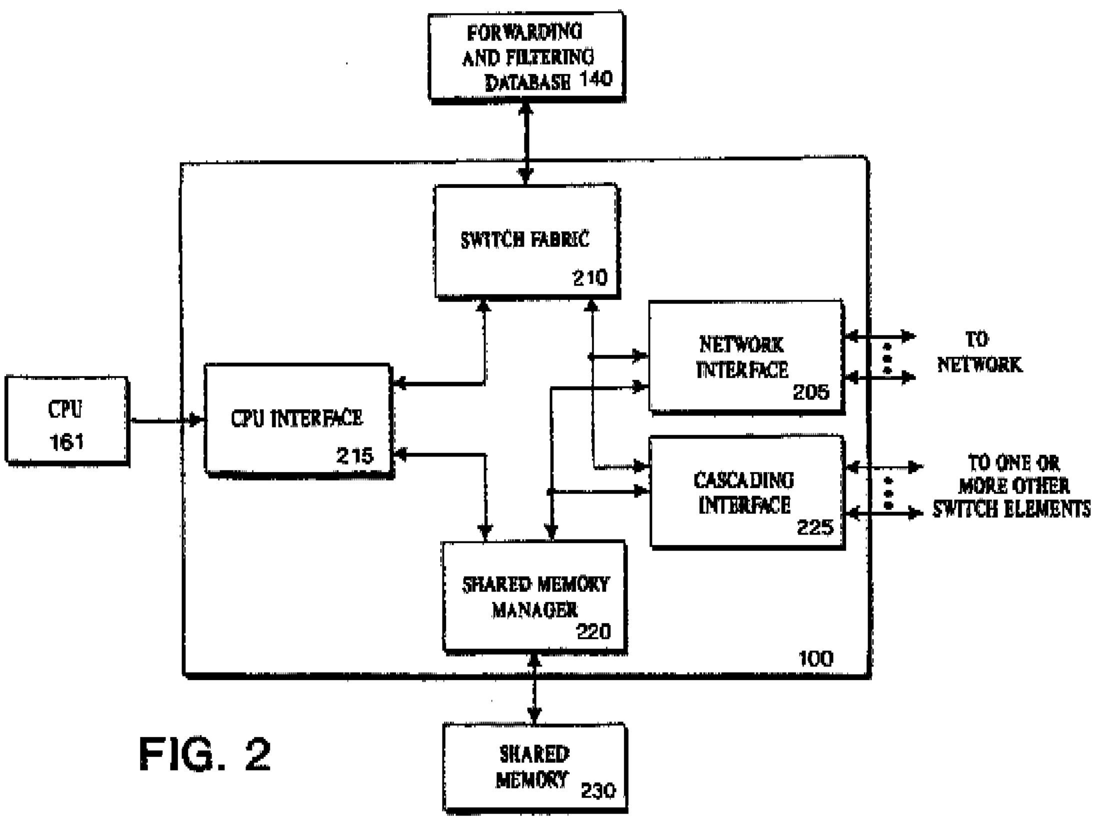


FIG. 2

Like Mathur, no regard is given to the destination specified within a packet when buffering the packet. The only relevant difference between the two references is that,

unlike Mathur, Muller makes use entirely of external memory, i.e., external shared memory 230, to buffer all packets flowing between any of the network interfaces 205. For example, col. 1, ll. 41-60 of Muller states:

> *Input packet processing includes the following: (1) receiving and verifying incoming Ethernet packets, (2) modifying packet headers when appropriate, (3) requesting buffer pointers from the shared memory manager 220 for storage of incoming packets, (4) requesting forwarding decisions from the switch fabric block 210, (5)* ***transferring the incoming packet data to the shared memory manager 220 for temporary storage in an external shared memory 230****, and (5) upon receipt of a forwarding decision, forwarding the buffer pointer(s) to the output port(s) indicated by the forwarding decision. Output packet processing may be performed by one or more output ports of the network interface 205. Output processing includes* ***requesting packet data from the shared memory manager 220****, transmitting packets onto the network, and requesting deallocation of buffer(s) after packets have been transmitted. (emphasis added).*

Thus, Muller teaches a switch in which an external shared memory 230 is used to buffer all packets flowing in between network interfaces 205. No controller determines destinations of packets received from the same interface and then buffers the packets differently based on the respective destinations.

As a result, Mathur in view of Muller fails to teach or suggest a routing component in which data (e.g., packets) received on the same interface may be buffered differently, i.e. using either internal or external memory, based on the particular destination of the packet. For these reasons, neither Mathur nor Muller, either singularly or in combination, teach or suggest a routing component having a controller that buffers data received from a network via a first interface using the embedded memory internal to the routing component when a destination of the data requires forwarding the data to a second one of the routing components using the crossbar arrangement, and buffers the data received from the network via the first interface in the external memory when the destination requires forwarding the data to the network, as required by claim 1.

Moreover, the combination of references fails to even teach or suggest a routing component that utilizes two different types of memory (embedded memory and external, off-chip memory), for buffering of packets. As described above, Mathur specifically teaches the use of an embedded memory for buffering <u>all</u> data. Similarly, Muller teaches use of a shared memory for buffering <u>all</u> data. Modification of Mathur in view of Muller

would result in use of a different memory type (i.e., external memory) to buffer packets in Mathur, but nevertheless use of external memory for all packets. Thus, neither Mathur nor Muller, either singularly or in combination, provide a suggestion of a routing component that utilizes two different types of memories, and a controller that buffers data from the same interface differently depending upon the destination of the packets in accordance with a forwarding table, as required by claim 1.

Response to the Examiner's Answer

In the Examiner's Answer, the Examiner's only response to Appellant's argument was to: (1) assert that the Appellant argued that "Mathur and Muller fail to disclose the use of [sic] buffering packets differently based on the destination specified within the packets and the bandwidth differences between the interfaces," and (2) maintain the rejection based solely on the premise that the claim 1 does not require bandwidth differences.[3]

This is a mischaracterization of Appellant's argument as a whole and avoids the issues raised with Appellant's Appeal Brief. Applicant acknowledges that claim 1 does not recite any limitations with respect to bandwidth. However, as set forth above, Appellant has discussed at length numerous deficiencies with of the rejection based on the combination of Mathur in view of Muller.

Specifically, Appellant discussed at length that fact that Mathur in view of Muller fail to teach or suggest a routing component in which a controller receives data (e.g., packets) from an interface, accesses forwarding information, and then buffers the packets differently, i.e. using either internal or external memory, based on the particular destination of each of the packets. In the Examiner's answer, the Examiner did not even comment on the deficiency in the rejection with respect to the literal elements of claim 1 that require a routing component having a controller that, based on a network destination for data received from an interface, buffers that particular data using either embedded memory internal to the integrated circuit when the destination requires forwarding the

[3] Examiner's Answer at pp. 10-11.

data to the second routing component of the router using the switch, or external memory when the destination requires forwarding the data to the network via the first interface.

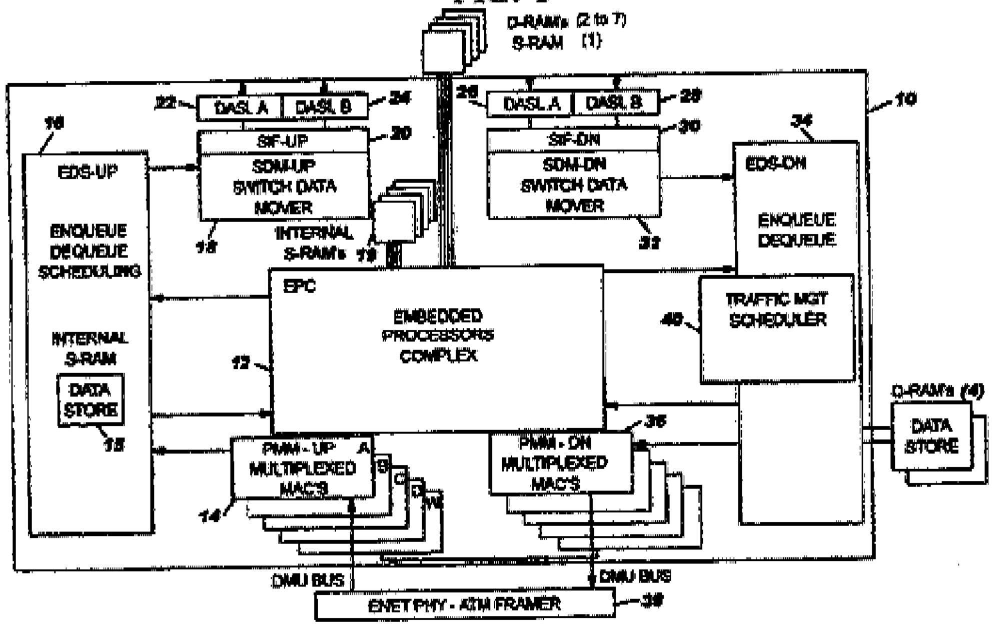
The Second Ground of Rejection

In the Examiner's Answer, the Examiner raised a new grounds of rejection and rejected claims 1-9, 11-20, 22-26, 28-32 and 34-35 rejected under 35 U.S.C. 102(e) as being anticipated by Bass et al. (USPN 6,460,120). With respect to the second ground of rejection, Appellant argues claims 1-9, 11-20, 22-26, 28-32 and 34-35 as a group, as set forth below. Again, Appellant directs the Board to independent claim 1.

As explained above, claim 1 requires at least one control unit that receives data from the network via the first interface and accesses a forwarding table to determine a network destination for the data. Claim 1 requires that the control unit buffer the data using the embedded memory internal to the integrated circuit when the destination requires forwarding the data to the second routing component of the router using the switch. In addition, claim 1 requires that the control unit buffer the data in the external memory when the destination requires forwarding the data to the network via the first interface. As explained in detail above, the literal language of claim 1 thus requires a routing component in which data received from the network on the **same** **interface (e.g., inbound packets from WAN interface 14) are buffered differently by using either embedded memory or external memory based on the particular destination to which the data is to be forwarded.** Bass fails to anticipate or suggest such a routing element.

Bass describes an interface device chip having internal memory (15) and external memory (DRAM 4), as shown in FIG. 1 reproduced below:

FIG. 1



Accoring to Bass, the arrows of FIG. 1 illustrate the data flow through the chip. (Bass at col. 7, ll. 23-24) Consistent with the arrows, Bass makes clear that **all** ingress traffic (traffic received from the Ethernet interface 38 located at the bottom of FIG. 1) is received by MAC's 14 and stored within internal S-RAM 15. (Bass at col. 7, ll. 25-26) Bass also makes clear that **all** egress traffic (traffic flowing downward and out the Ethernet interface 38) is stored within egress / external DRAM without basing any buffering decision on the particular destination.

Specifically, Bass clearly states that **all** inbound frames are stored within the internal memory 15 without any regard to the destination of the frames:

> *The arrows show the general flow of data within the Interface device. Frames received from an Ethernet MAC are placed in internal Data Store buffers by the EDS-UP.* (Bass at col. 7, ll. 25-26)

Similarly, Bass also clearly states that **all** outbound frames are stored in egress / external data store without any regard to the destination of the frames:

> *Frames received from the switch fabric are placed in Egress Data Store (Egress DS) buffers by an Egress EDS (34) and enqueued to the EPC.* (showed coupled to 4 external D-RAMS in FIG. 1) (Bass at col. 8, ll. 46-48).

Bass fails to teach or suggest a routing component in which data (e.g., a packet) received on the **same** interface is buffered differently, i.e. using either internal or external memory, based on the controller's determination of the particular destination of the data (i.e., the packet). That is, Bass fails to teach or suggest a routing component having a controller that accesses a forwarding table to first determine a network destination for data received from an interface, and then determines whether to buffer the data using the embedded memory internal to the integrated circuit or the external memory based on the destination, as required by claim 1. No controller or other structural component in Bass performs these functions.

The Bass controller does not utilize the destination of a packet to determine how a particular frame received from an interface should be buffered. In fact, quite the contrary to Appellant's claimed invention, all frames received from an interface are buffered exactly the same way. In Bass, all ingress frames received from the Ethernet interface are buffered using internal memory without regard to destination, and all egress frame received from the switch fabric are buffered using external memory without regard to destination.

For at least these reasons, Bass fails to anticipate or even suggest a routing element having a control unit that accesses a forwarding table to determine a network destination for data received from an interface and then: (1) buffers the data using the embedded memory internal to the integrated circuit when the destination requires forwarding the data to the second routing component of the router using the switch, and (2) buffers the data in the external memory when the destination requires forwarding the data to the network via the first interface, as required by claim 1.

To be clear, claim 1 requires at least one control unit that receives *data* from the network via the first interface and accesses a forwarding table to determine a network destination for the data. Claim 1 further requires that the control unit buffers *the data* using the embedded memory internal to the integrated circuit when the destination requires forwarding the data to the second routing component of the router using the switch. Claim 1 also requires that the control unit buffers *the data* in the external memory when the destination requires forwarding the data to the network via the first interface. This language provides clear and literal linkage between the data, the

destination for the data, and the buffering of the data. Thus, when viewed properly, claim 1 makes clear that the data referred to in the claim is received from one interface (the first interface), and the control unit accesses a forwarding table to determine the network destination for that same data. The subsequent language of claim 1 also makes clear that the control unit then buffers that same data (i.e., the data received from the first interface) in either in an internal buffer or an external memory based on the destination for that same data as determined from the forwarding table.

Bass fails to anticipate or even suggest these elements. In Bass, data received from the Ethernet interface is always buffered using the internal memory. For example, Bass describes no option for buffering the ingress data received from the Ethernet interface differently other than by using the internal memory. Bass provides no teaching or suggestion of a control unit that selects between internal and external memory to buffers the ingress data from the Ethernet interface based on the particular destination for the ingress data. To this extent, the Bass router operates substantially different and does not suggest all of the elements required by the routing element recited by Appellant's claim 1.

Conclusion of Arguments

The Examiner erred in rejecting Appellant's claims under 35 U.S.C. 103(a) as being unpatentable over Mathur (USPN 6,424,658) in view of Muller et al. (USPN 6,245,680). The Examiner also erred in raising the new grounds for rejection of claims 1-9, 11-20, 22-26, 28-32 and 34-35 rejected under 35 U.S.C. 102(e) as being anticipated by Bass et al. (USPN 6,460,120).

Reversal of the rejections and allowance of the pending claims are requested.

Respectfully submitted,

Date: May 8, 2007

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APPENDIX: CLAIMS ON APPEAL

Claim 1 (Previously Presented): A routing component of a router comprising:

a first interface to communicate data with a network;

a second interface to communicate data to a second routing component using a switch internal to the router, wherein the first interface and the second interface are integrated within a single integrated circuit;

an embedded memory within the integrated circuit;

a memory interface to couple the integrated circuit to an external memory; and

at least one control unit that receives data from the network via the first interface and accesses a forwarding table to determine a network destination for the data;

wherein the control unit buffers the data using the embedded memory internal to the integrated circuit when the destination requires forwarding the data to the second routing component of the router using the switch, and

wherein the control unit buffers the data in the external memory when the destination requires forwarding the data to the network via the first interface.

Claim 2 (Previously Presented): The routing component of claim 1, wherein the at least one control unit comprises:

a first control unit to buffer in the embedded memory data that is received from the first interface and forwarded to the second interface; and

a second control unit to buffer in the external memory data that is received from the second interface and forwarded to the first interface.

Claim 3 (Original): The routing component of claim 2, wherein the external memory has a greater storage capacity than the embedded memory.

Claim 4 (Original): The routing component of claim 1, wherein the first interface comprises a wide area network (WAN) interface.

Claim 5 (Original): The routing component of claim 1, wherein the second interface comprises a switch fabric interface.

Claim 6 (Original): The routing component of claim 5, wherein the switch fabric interface communicates crossbar data.

Claim 7 (Previously Presented): The routing component of claim 1, wherein the routing component is implemented using a single application specific integrated circuit (ASIC).

Claim 8 (Original): The routing component of claim 1, wherein the embedded memory comprises a random access memory (RAM).

Claim 9 (Previously Presented): A network element comprising:

a first network interface to communicate data with a network;

a second network interface to communicate data with the network;

a routing component formed in an integrated circuit, wherein the routing component has an embedded memory within the integrated circuit; and

a second memory external to the routing component,

wherein the routing component receives data from the first network interface and accesses a forwarding table to determine a network destination for the data,

wherein the routing component buffers data in the embedded memory internal to the routing component when the destination requires forwarding the data to a second routing component using a switch internal to the network element, and

wherein the routing component buffers data communicated in the second memory external to the routing component when the destination requires forwarding the data to the network via the first network interface.

Claim 10 (Cancelled).

Claim 11 (Previously Presented): The network element of claim 9, wherein the second memory has a greater storage capacity than the embedded memory.

Claim 12 (Previously Presented): The network element of claim 9, wherein the first network interface and the second network interface comprise wide area network (WAN) interfaces.

Claim 13 (Previously Presented): The network element of claim 9, further comprising a crossbar switch fabric coupling the routing component to a second routing component.

Claim 14 (Previously Presented): The network element of claim 13, wherein the switch fabric communicates crossbar data.

Claim 15 (Previously Presented): The network element of claim 9, wherein the routing component is implemented using an application specific integrated circuit (ASIC).

Claim 16 (Original): The network element of claim 9, wherein the embedded memory comprises a random access memory (RAM).

Claim 17 (Previously Presented): The network element of claim 9, wherein the second routing component includes an embedded memory to store data communicated using the second network interface.

Claim 18 (Previously Presented): An integrated circuit (IC) comprising:

a first interface to communicate data with a network at a first data rate;

a second interface to communicate data with a switch fabric at a second data rate higher than the first data rate;

an embedded memory internal to the IC;

an interface to a memory external to the IC; and

at least one control unit that receives data from the first interface and accesses a forwarding table to determine a network destination for the data,

wherein the control unit buffers data in the embedded memory internal to the integrated circuit when the destination requires forwarding the data using the switch fabric, and

wherein the control unit buffers the data using the external memory when the destination requires forwarding the data out to the network via the first interface.

Claim 19 (Original): The IC of claim 18, wherein the memory external to the IC has a greater storage capacity than the embedded memory.

Claim 20 (Original): The IC of claim 18, wherein the first interface is coupled to a wide area network (WAN) interface.

Claim 21 (Cancelled).

Claim 22 (Previously Presented): The IC of claim 18, wherein the switch fabric comprises a crossbar.

Claim 23 (Original): The IC of claim 18, wherein the embedded memory comprises a random access memory (RAM).

Claim 24 (Previously Presented): A router comprising:

an integrated circuit (IC) comprising:

a first interface to communicate data with a network;

a second interface to communicate data with a switch fabric internal to the router;

an embedded memory; and

an interface to a memory external to the IC; and

at least one control unit that receives data from the network via the first interface and accesses a forwarding table to determine a network destination for the data,

wherein the control unit buffers the data using the embedded memory internal to the integrated circuit when the destination requires forwarding the data to a routing component of the router using the switch fabric, and

wherein the control unit buffers the data in the external memory when the destination requires forwarding the data to the network via the first interface.

Claim 25 (Original): The router of claim 24, wherein the memory external to the IC has a greater storage capacity than the embedded memory.

Claim 26 (Original): The router of claim 24, wherein the first interface is coupled to a wide area network (WAN) interface.

Claim 27 (Cancelled).

Claim 28 (Previously Presented): The router of claim 24, wherein the switch fabric comprises a crossbar.

Claim 29 (Original): The router of claim 24, wherein the embedded memory comprises a random access memory (RAM).

Claim 30 (Previously Presented): A method for communicating data using a network router, the method comprising:

receiving inbound data from a network interface via a first routing component;

accessing a forwarding table with a control unit of the network router to determine a network destination for the data;

when the destination requires forwarding the data to a second routing component internal to the router using a switch having a higher bandwidth than the network interface, buffering the inbound data within an embedded memory internal to the first routing component;

forwarding the inbound data from the first routing component to a second routing component via the switch;

receiving outbound data with the first routing component from the switch;

when the destination requires forwarding the outbound data to the network interface having a lower bandwidth than the switch, buffering the outbound data within a memory external to the first routing component; and

forwarding the outbound data to the network interface.

Claim 31 (Previously Presented): The method of claim 30, wherein the external memory has a greater storage capacity than the embedded memory.

Claim 32 (Previously Presented): The method of claim 30, wherein the first network interface comprises a wide area network (WAN) interface.

Claim 33 (Canceled).

Claim 34 (Previously Presented): The method of claim 30, wherein the switch communicates crossbar data.

Claim 35 (Previously Presented): A routing arrangement comprising:

a crossbar arrangement;

a plurality of routing components coupled to the crossbar arrangement, at least a first one of the routing components comprising:

a first interface to communicate data with a network;

a second interface to communicate data with the crossbar arrangement;

an embedded memory;

an external memory interface to a memory external to the routing component; and

at least one control unit that receives data from the first interface and determines a network destination for the data,

wherein the control unit buffers the data using the embedded memory internal to the routing component when the destination requires forwarding the data to a second one of the routing components using the crossbar arrangement, and

wherein the control unit buffers the data in the external memory when the destination requires forwarding the data to the network via the first interface.

APPENDIX: EVIDENCE

None

APPENDIX: RELATED PROCEEDINGS

None